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# USB 2.0 High Speed 7-Port Hub Controller

## Introduction

The FE2.1 is a highly integrated, high quality, high performance, low power consumption, yet low overall cost solution for USB 2.0 High Speed 7-Port Hub.

It adopts Multiple Transaction Translator (MTT) architecture to explore the maximum possible throughput. Six, instead of two, non-periodic transaction buffers are used to minimize potential traffic jamming. The whole design is based on state-machine-control to reduce the response delay

**FE 2.1**

**USB 2.0 High Speed 7-Port Hub Controller**

To guarantee high quality, the whole chip is covered by Test Scan Chain – include even the high speed (480MHz) modules, so that all the logic components could be fully tested before shipping. Special Build-In-Self-Test mode is designed to exercise all high, full, and low speed Analog Front End (AFE) components in the packaging and testing stages as well.

Low power consumption is achieved by using 0.18µm technology and comprehensive power/clock control mechanism. Most part of the chip will not be clocked unless needed.

**Evaluation-Board**

**available**

-40°C - 85°C

**FE2.1 7-Port USB Hub**
**Extended Temperature Range**

Order No. LQFP-48 (7x7mm Tray)
Order No. CQFP48ATR (7x7mm Tape & Reel)

## Features

- Low power consumption
  - 155 mA when seven downstream facing ports enabled in High-Speed mode
  - 66 mA when one downstream facing port enabled in High-Speed mode
- Fully compliant with Universal Serial Bus Specification Revision 2.0 (USB 2.0)
- Upstream facing port supports High-Speed (480MHz) and Full-Speed (12MHz) modes
- 7 downstream facing ports support High-Speed (480MHz), Full-Speed (12MHz), and Low-Speed (1.5MHz) modes
- Integrated USB 2.0 Transceivers
- Integrated upstream 1.5KΩ pull-up, downstream 15KΩ pull-down, and serial resisters
- Integrated 5V to 3.3V and 1.8V regulator
- Integrated Power-On-Reset circuit
- Integrated 12MHz Oscillator with feedback resister, and crystal load capacitator
- Integrated 12MHz-to-480MHz Phase LockLoop (PLL)
- Multiple Transaction Translators (MTT)
  - One TT for each downstream port
  - Alternate Interface 0 for Single-TT, and Alternate Interface 1 for Multiple-TT
  - Each TT could handle 64 periodic Start-Split transactions, 32 periodic Complete-Split transactions, and 6 none-periodic transactions
- Support Self-Powered Mode only
- Board configured options –
  - Ganged or Individual Power Control Mode select
  - Global, Multiple Ganges, or Individual Over-Current Protection Mode select
  - Removable or Non-Removable Downstream Devices configuration
  - Number of Downstream Ports
- EEPROM configured options:
  - Vendor ID, Product ID, & Device Release Number
  - Removable or Non-Removable Downstream Devices configuration
  - Serial Number
  - Number of Downstream Ports
- Comprehensive status indicators support:
  - Standard downstream port status indicators (Green and Amber LED control for each downstream port)
  - Hub active/suspend indicator LED

Subject to change without notice

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